Savas Kaya

Birth Place:	Istanbul	Address:	School of EE&CS, 361 Stocker Center
Date of Birth:	20 May 1971		Ohio University, Athens OH 45701
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EDUCATION

Post-Graduate	1994-1998	***PhD in Semiconductor Device Electronics.*** **Imperial College of Science, Technology & Medicine, University of London.** *Thesis:* Electrical Transport in Strained Silicon Quantum Wells on Vicinal Substrates. Researched into the physics and application of novel Si/SiGe heterojunctions on flat and tilted substrates, using full range of advanced nanoelectronic design, fabrication and measurement tools.
	1993-1994	***MPhil in Semiconductor Physics & Microelectronic Engineering.*** **Darwin College, University of Cambridge.** *Thesis:* Liquid Crystal Polarisation Insensitive Liquid Crystal Switches for Optical Arrays. Taught course focused on the theory and application of novel microelectronic and optoelectronic devices and semiconductor materials.
Undergraduate	1988-1992	***BSc Hons. in Electronic & Communication Engineering.*** **Department of Electronics and Communication, Istanbul Technical University.** 73.6% average—11th in graduation ranking. Opted in the final year for *Microelectronics* package with a strong emphasis on analogue and digital VLSI design.

WORK EXPERIENCE

2010 ***Visiting Professor,*** **Dept of Electrical and Computer Engineering, University of California Davis**
Collaborative research for 8 months with Prof. Saif Islam's group, primarily focusing on the use of nanowires and nanostructured materials for low-voltage corona generation in air filtering and cooling applications.

2007-Present ***Associate Professor,*** **School of Electrical Engineering and Computer Science, Ohio University.**
2001-2007 ***Assistant Professor,*** **School of Electrical Engineering and Computer Science, Ohio University.**
Teaching and carrying out research in novel semiconductor and nanostructured materials, fabrication processes, devices, characterization techniques.

Instructor for the following courses:

EE102 Intr. to Digital Design	EE103 Intr. to Electronic and Computer Eng
EE334 Intermediate Electronics II	EE395 Intermediate Electronics Lab B
EE371 Probability & Statistics	EE418 Micro-Nano Fabrication
EE415 VLSI Design I	EE495 Capstone Design Project
EE520 Nanoelectronics & Nanotechnology	EE690 Advanced Semiconductor Devices

1998-2001 ***Post-doctoral Researcher*****, Nanoelectronics Research Centre, University of Glasgow.**
Worked in independent and team-oriented research projects mainly on the numerical modeling and down scaling of MOSFET architecture using Si/SiGe material as well as techniques for RF and low-power circuitry. Also took part in research into 'atomistic' simulations of fluctuation phenomena in ultra-small MOSFETs. Employed a wide range of numerical tools in modeling of semiconductor below 100 nm including traditional drift-diffusion, energy, balance or hydrodynamic models, and advanced Monte Carlo particle simulation techniques. Also involved in teaching, research planning and grant applications.

1996-1997 ***Teaching Assistant,*** **University of London, Imperial College of Science, Technology & Medicine.**
Demonstrated experiments for *Electronics Laboratory II*. Experiments covered AD/DA converters, diode and transistor switching, DSP using Matlab©, analogue control, modulation techniques and amplifiers.

1992-1993 ***Research & Teaching Assistant*****, Istanbul Technical University.**
Engaged with research into *Capacitive Threshold Logic* and taught as course tutor for *Electronics I*.

RESEARCH GRANTS

Baker Award	$10,000 Completed	*PI,* Breakdown of Universal Mobility Behavior in decanano MOSFETS, July 2002.
Stocker Faculty Enrichment	$2,700 Completed	Support for travel & conference attendances, June 2004, June 2005, June 2010
Ohio Univ. TTO & RCENT	$12,000 Completed	*PI,* 3D Study of COSMOS Architecture, February 2005.
Ohio Univ. BNNT	$25k Completed	*Co-PI*: STM Analysis of Transmembrane Proteins: Case for Na/K ATPase, June 2006
AFRL - Wyle Labs	$15k Completed	*PI, A Feasibility Study: DG-MOSFET Reconfigurable Systems*, November 2006.
Ohio Univ. BNNT	$25k Completed	*PI*: An interdisciplinary Study of Structure & Function in Trans-membrane Proteins, June 2007-2009
DARPA, SBIR Phase 1	$33k Completed	*Co-PI/Subcontractor*: Tunable Analog Circuits with DG-MOSFETs, February 2009-July2009.
NSF	$300k Completed	*PI*, EMT: *Study of Transmembrane Proteins for Biomolecular Logic & Storage,* July 2006.
ODOT	$40k Completed	*Co-PI: The Use of Atomic Force Microscopy to Evaluate Warm Mix Asphalt*, Sep 2011-2012
Ohio Univ. GERB	$845k Ongoing	*Co-PI*: *Nanoscale & Quantum Phenomena Institute: GERB Proposal for International Prominence*, July 2008-2013.
1804 Fund	$80k Ongoing	*PI: Enhancement of MOCVD Material Growth System for Advancement of Campus-Wide Research and Education in Nanomaterials and Nanodevices*
NSF	$380k Ongoing	*Co-PI: Power-Efficient Reconfigurable Wireless Network-on-Chip (NoC) Interconnects for Future Many-core Architectures*, Sep 2011-2014
NSF	$1.3M Ongoing	*Co-PI: MRI: Acquisition of Transmission Electron Microscope for Advanced Materials Relating to Energy Storage, Alternative Energy, Remediation, and Superconductors*, Oct 2011-2014
NSF	$200k Ongoing	*PI: NUE – NanO StUdio* An Immersive Ambience for Nano Educational Experiences, January 2012
ODOT	$81k Ongoing	*Co-PI: Influence of Warm Mix Asphalt on Aging of Asphalt Binders*, Aug 2012-Dec 2014
NSF	$600k Ongoing	*Senior Staff: ACE: Appalachian Cohort for Engineering*, July 2012-2015
1804 Fund	$70k Ongoing	*PI: nan**O**-st**U**dio: An Interactive Undergraduate Laboratory of Nanotechnology to Enhance Research and Outreach in Ohio University,* 2012-2014
RCENT	$60k Ongoing	*Co-PI: Production of Bioasphalt from Sustainable Feedstocks via Catalytic Pathways*, Sep 2012-13
NSF	$297k Pending	*Co-PI: Conductive Asphalt Nanocomposites: A Path for Smart & Sustainable Pavements*, Oct 2012
NSF/NIH	$500k Planned	*PI: Artificial Membranes on Nanoporous Alumina for Lab-on-a-Chip Applications and Single Protein Measurements.*

HONORS & AWARDS

1988	173rd among 650,000 candidates of Turkish National University Selection Examination.
1993-1998	Turkish Ministry of Education MSc and PhD Scholarship for UK.
2001	Invited and partially-funded participant to Quantum Transport Workshop, Maratea, Italy, 17-22 June 2001.
2004	Departmental Best Teacher Award: Represented School of EE&CS in the RCENT Awards.
2005	Invited and partially-funded participant to Summer School on *Mechanisms Of Membrane Transport*, Tilton, NH, 5-10 June 2005

2005	Recipient of Russ College Martin E. and Ann D. White Research Paper Award.
2006	Promotion to Senior Membership of IEEE in recognition of 10 years service to the profession
2006-2008	Air Force Summer Faculty Fellow
2011	Departmental Best Paper Award: Represented School of EE&CS in the RCENT Best Paper Award.

GRADUATE ADVISEES

Nov 2000	Yinpeng Zhao (co-advised), PhD Dissertation: "Simulation and Optimisation of SiGe MOSFETs"
Sep 2001	David Magot (co-advised), MSc Thesis: "Analysis of Line Edge Roughness for Device Simulations"
Feb 2004	James Fonseca, MS Thesis: "Accurate Treatment of Interface Roughness in Nanoscale Double-Gate MOSFETs using Non-Equilibrium Green's Functions"
Apr 2004	Rameshwari Chinchani, MS Thesis: "Strained Si/SiGe Heterostructure CMOS Devices: A Simulation Study of Linearity"
July 2004	Wei Ma, MS Thesis:,"Linearity Analysis of Single and Double-Gate SOI MOSFETs"
Nov 2005	Swetha Varadharajan, MS Thesis: "Analog and Digital Applications of DG-MOSFETs"
Apr 2006	Ahmad al-Ahmadi, PhD Dissertation: "COSMOS: A Novel Nanoscale CMOS Architecture"
Jun 2008	James Fonseca, PhD Dissertation: "Temporal & Steric Analysis of Ionic Permeation and Binding in Na+,K+-ATPase via Molecular Dynamics Simulations
Sep 2008	Darwin T. Ting, MS Thesis: "Reconfigurable Threshold Logic Gates Implemented in Nanoscale Double-Gate MOSFETs"
Jan 2009	Anish Kulkarni, MS Thesis: "Study of Tunable Analog Circuits Using Double Gate Metal Oxide Semiconductor Field Effect Transistors"
Jun 2010	Sunny Mishra, MS Thesis: "Simulation & Modeling of Ion-Transporting Membrane Proteins"
Aug 2010	Kendal Clark, PhD Dissertation: "STM Study of Molecular and Biomolecular Electronic Systems"
Sep 2010	Ravikiran Vuppuluri, MS Thesis: "Electrochemical Growth of Nanoporous Alumina Membranes and its Applications"
Nov 2011	Harshita Dasari, MS Thesis: "Microsphere Lithography: A Low Cost Next Generation Lithography for Nanodevice Fabrication"
Jun 2013*	Isha Shrivastava, MS Candidate: "Fabrication and Characterization of Platinum NanoComb Structures for Electrochemical Cells"
Sep 2013*	Jason Wright, MS Candidate: "Design and Development of High Accuracy Instrumentation for Nanosensor Characterization"
Dec 2013*	Soumyasanta Laha, PhD Candidate: "Feasibility of Si CMOS mm-Wave Technology for WiNoCs "
Dec 2017*	Parthiban Rajan, PhD Candidate: "Opto-Fluidic Channels for co-Transfer of Heat and Data in Nanochips "

*Provisional

PROFESSIONAL SERVICE

2000	Served as a member of Local Organizing Committee of IWCE7—7th International Workshop in Computational Electronics, which was held in Glasgow from 22-25 May 2000.
2002-present	Active reviewer for the following professional journals: Solid-State Electronics, IEEE Transactions in Electron Devices, Electronic Letters, IEEE Transactions in Nanotechnology, IET Devices, Circuits & Systems, ETRI
2003	Invited for NSF Review Panels
2006	Served as a member of Local Organizing Committee of IEEE Nanotech—*6th International IEEE Nanotechnology Conference*, which was held in Cincinnati, USA, from 17-20 July 2006.
2007	Served as a member of Program Committee for SPIE Photonics East Symposia: *Nanophotonics for Communication (IT407) & Nanomaterials (SA114)*, held in Boston, USA, from 9-12 September 2007.
2009	Served as a member of Program Committee for SPIE Optics and Photonic Meeting, *Nanoepitaxy: Synthesis, Characterization and Device Integration of Nanomaterials*, San Diego, USA, August 2009.

2010	Served as a member of Program Committee for *Micro-Nanotechnology Sensors, Systems, and Applications Conference*, held in Orlando, Florida, USA, May 2011.
2011	Invited for NSF Review Panels (twice in 2011)

COMMITTEES SERVED

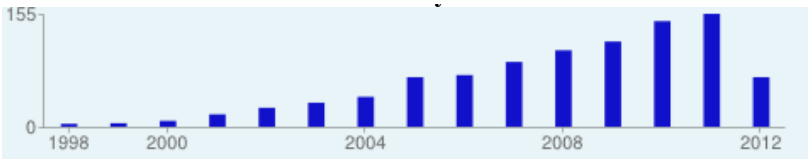
Thesis & Dissertations	2001-Present	*Served in +34 MS Thesis & +18 PhD Dissertation Committees*, including students from the following departments: Electrical Engineering & Computer Science, Industrial Systems & Engineering, Chemical & Biomolecular Engineering, Mechanical Engineering, Civil Engineering, Physics & Astronomy, School of Film.
School of EE&CS	2001-2003	*Space Planning; UG Recruitment; Research; Assessment & Accreditation*
	2004-2005	*UG Recruitment; Research; ABET Accreditation*
	2006	*Graduate; UG Recruitment & ABET Accreditation*
	2007-2008	*Promotion & Tenure; Graduate; UG Recruitment*
	2009-2010	*Curriculum, Recruitment & ABET*
	2011-present	*Graduate, Space Planning, Recruitment*
Russ College of Eng & Tech	2001-2003	*Library, NQPI/CMSS Liason*
	2004-2005	*Library, NQPI/CMSS Liason*
	2006-2009	*Integrated Eng PhD Steering; BioMedical Eng Steering; NQPI/CMSS Liason*
	2011-present	*Center for Electrochemical Research Steering; IT Technology; NQPI/CMSS Liason*
Ohio Univ.	2004-2005	*Faculty Senate (Substitute Member)*
	2010-present	*Council for Research, Scholarship and Creative Activity (CRESCA)*

PERSONAL

Leadership	2001-Present	*Faculty Advisor,* Ohio University Turkish Student Association.
	2004-Present	*Faculty Advisor,* IEEE Ohio University Athens Student Chapter.
	1996-1998	*President,* Imperial College Turkish Society. Represented and administered the society in national and international events.
Skills	Languages	Fluent and proficient in Turkish & English
	Computers	Experienced user on and capable of administration of computers running *Linux/Unix, Windows* and *MacOS* operating systems. Programming in Pascal, FORTRAN and HTML
	Software	Expert user in common desktop publishing and office utility programs. Advanced user of *Synopsis ECAD/TCAD* tools, including DESIS, DIOS, MEDICI, TSUPREM. Experience with ECAD tools by CADENCE and Mentor Graphics. Extensive and advanced user of general scientific tools such as MATLAB, Mathematica, XMGR, LaTeX *etc.*
Continuous Professional Development	*Current Mode Circuits,* Continuing Education Centre, Imperial College, London, 8-10 Jul 1996.	
	Speaking Technically: Workshop A, Dept. of Humanities, Imperial College, London, 17-18 April 1997.	
	Mentoring: Working with Small Groups, Teaching& Service, University of Glasgow, 1st Oct 1999.	
Membership	Have affiliation with the following professional organizations *IEEE, SPIE*	
Interests	Travel, reading on science, philosophy and mysticism, cinema & air shows, chess. Sports: basketball, European soccer and squash	

CITATION STATISTICS (SCHOLAR.GOOGLE.COM)

	All	Since 2007
Citations	967	680
h-Index	11	9
i-10 Index	13	9



PUBLICATIONS

Theses:

1. "Polarisation Insensitive Liquid Crystal Switches for Optical Arrays", *MPhil, University of Cambridge*, 1994.
2. "Electrical Transport in Strained Silicon Quantum Wells on Vicinal Substrates", *PhD, Imperial College -University of London*, 1999.

Book Chapters:

1. "Atomistic Simulation of Decanano MOSFETs" , A Asenov, A R Brown and **S Kaya**, in *"Predictive Simulation of Semiconductor Processing: Status and Challenges",* Eds. J. Dabrowski & E. R. Weber, Springer, Berlin, pp.111-156 (2004).
2. "Tunable Analog and Reconfigurable Digital Circuits with Nanoscale DG-MOSFETs", **S Kaya**, H F A Hamed and S Laha in *"Advances in Analog Circuits",* Ed. E. Tlelo-Cuautle, INTECH Open Access, Vienna, ISBN: 978-953-307-323-1, pp.181-209 (2011).

Refereed Journals:

1. "Using AFM To Study The Viscoelastic Behavior Of Asphalt Binders", M Nazzal, **S Kaya**, and L. Abu-Qtaish in preparation for submission to *Journal of Construction and Building Materials, Elsevier*.

2. "Channel Modeling for Wireless Networks-on-Chips", D W. Matolak, A Kodi, and **S Kaya**, in preparation for submission to *IEEE Journal of Communications,* 2012.

3. "A-WiNoC: Adaptive Wireless Network-on-Chip Architecture Using Energy-Efficient Transceivers", D DiTomaso, A Kodi, D W. Matolak, **S Kaya**, S Laha, and W Rayess, submitted to *IEEE Trans. CAD*, 2012.

4. "UV and Oxygen Sensing Properties and Space Charge Limited Transport of Sonochemically Grown ZnO Nanowires", A P Nayak, T-C Lin, D Lam, S Kaya, M. S Islam, in print, *Nanoscience & Nanotechnology,* 2012.

5. "Fundamental Characterization of Nano-Clay Asphalt Composites", M. Nazzal, **S Kaya**, T Günay and P Ahmedzade, *ASCE Journal of Nanomechanics and Micromechanics,* in print*,* 2012

6. "Wireless Networks-on-Chips: Architecture, Wireless Channel, and Devices", D W. Matolak, A Kodi, **S Kaya**, D DiTomaso, S Laha, W Rayess, *IEEE Wireless Communications,* in print*,* 2012

7. "Electrochemically Grown Metallic Nanocomb Structures on Nanoporous Alumina Templates", **S Kaya** and E Atar, *Appl. Phys Lett*. vol.98, p.223105, 2011.

8. "Improved Reconfigurability and Noise Margins in Threshold Logic Gates via Back-Gate Biasing in DG-MOSFETs", **S Kaya**, H F A Hamed and D T Ting, *J Analog Integr. Circ. & Sig. Process*., vol.68, p.101. 2011.

9. "Growth of metallic nanowires on nanoporous alumina templates: Nanocomb Structures", E Atar, R V Vuppuluri and **S Kaya**, *Proceedings of SPIE,* vol. 7768, 77680S, 2010.

10. "Widely tunable low-power high-linearity current-mode integrator built using DG-MOSFETs", **S Kaya,** H F A Hamed and A Kulkarni, *J Analog Integr. Circ. & Sig. Process.*, ***62****(2), 215-222*, 2009, DOI 10.1007/s10470-009-9334-6.

11. "Learning Before Erring: A Brief Note on the Influence of Dielectric Materials to Pursue Moore's Law", W. A. Young II, S Kaya, and G R Weckman, *Int. J of Industrial Engineering - Theory, Applications and Practice, **16**(2), 91-98, 2009.*

12. "Use of nano-scale double-gate MOSFETs in low-power tunable current mode analog circuits", H F A Hamed, **S Kaya** and J Starzyk, *J Analog Integr. Circ. & Sig. Process.*, vol.54, p.211. 2008.

13. "Exploration of Na+,K+-ATPase Ion Permeation Pathways via Molecular Dynamic Simulation and Electrostatic Analysis", J. E. Fonseca, S. Mishra, **S Kaya** and R. F. Rakowski, *J Computational Electronics,* vol.7, p.20, 2008.

14. "Low-power tunable nanocircuits with DG-MOSFETs for current sensing applications, **S Kaya** and H F A Hamed, *Proceedings of SPIE*, vol.6769, 67690D, 2007.

15. "Reconfigurable Threshold Logic Gates with nano-scale DG-MOSFETs", **S Kaya**, H F A Hamed, D T Ting and G Creech, *Solid-State Electronics*, vol. 51, p. 1301, 2007

16. "Temporal and steric analysis of ionic permeation and binding in SERCA via molecular dynamic simulations", J. E. Fonseca, **S. Kaya** and R. F. Rakowski, *IOP Nanotechnology*, vol.18, p.424022, 2007, *for an on-line version visit:* http://www.iop.org/EJ/abstract/0957-4484/18/42/424022/

17. "Low-Power Tunable Analog Circuit Blocks Based on Nanoscale Dual-Gate MOSFETs", **S Kaya**, H F A Hamed and J Starzyk, *IEEE Trans Circ. & Sys II*, vol. 54, p. 571, 2007.

18. "Temporal Analysis of Valence & Electrostatics in Ion-Motive Sodium Pump", J E Fonseca, **S Kaya**, S Guennoun and R F Rakowski, *J Computational Electronics*, vol.6, p.381, 2007.

19. "Power•Delay Product in COSMOS Logic Circuits", A Al-Ahmadi and **S Kaya**, *J Computational Electronics*, vol.5, p.305, 2006.

20. "Electro-Chemical Modeling Challenges of Biological Ion Pumps", R F Rakowski, **S Kaya** and J E Fonseca, *J Computational Electronics*, vol.4, p.189, 2005.

21. "Search for Optimum and Scalable COSMOS", **S Kaya** and A Al-Ahmadi, *J Computational Electronics*, vol.4, p.119, 2005.

22. "RF Performance of Strained SiGe pMOSFETs: Linearity and Gain", W Ma and **S Kaya**, *J Computational Electronics*, vol.4, p. 269, 2005.

23. "COSMOS: A New MOS Device Device Paradigm", **S Kaya**, *IEEE Transactions Nanotechnology*, vol. 5, p. 588, 2005.

24. "Optimization of RF linearity DG-MOSFETs", **S.Kaya** and W Ma, *IEEE Electron Device Letters*, vol. 25, p. 308, 2004.

25. "Impact of device physics on DG and SOI MOSFET linearity", W Ma and **S.Kaya**, *Solid-State Electronics*, vol. 48, p. 1741, 2004

26. "Accurate treatment of interface roughness in nanoscale DG MOSFETs using non-equilibrium Green's functions", J E Fonseca and **S.Kaya**, *Solid-State Electronics*, vol. 48, p. 1843, 2004

27. "Study of RF Linearity in sub-50nm MOSFETs Using Simulations", W Ma, **S.Kaya** and A.Asenov, *J Computational Electronics*, vol.2, pp.347-352, 2003.

28. "Statistical Fluctuation of Universal Mobility Curves in sub-100nm MOSFETs due to Random Oxide Interface", **S Kaya**, *Physica Status Solidi (b)*, vol.239, p.110, 2003.

29. "Simulation of Intrinsic Parameter Fluctuations in Decananometre and Nanometre scale MOSFETs", A.Asenov, A.R.Brown, J.H.Davies, **S Kaya** and G.Slavcheva, *IEEE Transaction Electron Devices*, vol. 50, p. 1837, 2003.

30. "Intrinsic Parameter Fluctuations in Decananometre MOSFETs Introduced by Gate Line Edge Roughness", A Asenov, **S Kaya** and A R Brown, *IEEE Transaction Electron Devices*, vol. 50, p. 1254, 2003.

31. "Breakdown of Universal Mobility Curves in sub-100nm MOSFETs", **S Kaya**, A Asenov and S Roy, *IEEE Trans Nanotech.*, vol.1, p.260, 2002.

32. "On the Breakdown of Universal Mobility Curves in sub-100nm MOSFETs: A 3D Brownian Simulation Framework", **S Kaya**, S Roy and A Asenov, *J Computational Electronics*, p.375, 2002.

33. "Implications of Imperfect Interfaces and Edges in Ultra-small MOSFET Characteristics", A Asenov, **S Kaya** and A R Brown, *Physica Status Solidi (b)*, vol.233, p.101, 2002.

34. "Intrinsic Threshold Voltage Fluctuations in Decanano MOSFET's due to Local Oxide Thickness Variations" A Asenov, **S Kaya** and J H Davies, *IEEE Transaction Electron Devices*, vol. 49, p. 112, 2002.

35. "Quantum Corrections to the 'Atomistic' MOSFET simulations", A Asenov, G Slavcheva, **S Kaya** and R Balasubramaniam, *VLSI Design*, vol.13, p. 15, 2001.

36. "On the Mobility Extraction for HMOSFETs", U N Straube, A G Evans, G Braithwaite, **S Kaya**, J Watling and A Asenov, *Solid-State Electronics*, vol. 45, p. 527, 2001.

37. "Effective Mobilities in Pseudomorphic Si/SiGe/Si p-channel MOSFETs with thin silicon capping layers" M J Palmer, G Braithwaite, T J Grasby , P J Phillips, M J Prest, E H C Parker, T E Whall C P Parry, A M Waite, A G R Evans, S Roy, J R Watling, **S Kaya** and A Asenov. Applied Physics Letters, 78(10), p. 1424, 2001.

38. "Oxide Thickness Variation Induced Threshold Voltage Fluctuations in Decanano MOSFET's: A 3D Density Gradient Simulation Study", A Asenov, **S Kaya**, J H Davies and S Saini. *Superlattices & Microstructures*, vol. 28, No. 5/6, p. 507, 2000.

39. "RF Analysis Methodology for Si and SiGe FETs Based on Transient Monte Carlo Simulation" S Roy, **S Kaya**, A Asenov and J R Barker, *IEICE Transactions in Electronics*, vol. E83**-C**, p. 1224, 2000.

40. "Indication of Velocity Overshoot in strained Si0.8Ge0.2p-channel MOSFET's", **S Kaya**, Y-P Zhao, J R Watling, A Asenov, J R Barker, G Ansaripour, G Braithwaite, E H C Parker and T E Whall, *Semiconductor Science & Technology*, 15, p. 573, 2000.

41. "Drift Diffusion and Hydrodynamic Simulations of Si/SiGe p-MOSFETs", Y P Zhao, J R Watling, **S Kaya**, A Asenov and J R Barker Material Science & Engineering B, 72, p.180, 2000.

42. "MOS gated Si:SiGe quantum wells by anodic oxidation" J C Yeoh, P W Green, T J Thornton, **S Kaya**, K Fobelets and J M Fernández Semiconductor Science & Technology, 13, p.1442, 1998

43. "Si/SiGe quantum wells grown on vicinal Si(001) substrates: morphology, dislocation dynamics and transport properties", P Waltereit, J M Fernandez, **S Kaya** and T J Thornton, Applied Physics Letters, 72(18), p.2262, 1998.

44. "Evidence For Inter-Miniband Scattering Due to Electron Heating in Si:SiGe Quantum Wells grown on Tilted Substrates" **S Kaya**, T J Thornton, K Fobelets, P W Green and J M Fernandez, *Physica Status Solidi (b)*, 204, p.227, 1997.

45. "Si:SiGe Quantum wells grown on (118) substrates: surface morphology and transport properties", T J Thornton, J M Fernandez**, S Kaya**, P W Green and K Fobelets Applied Physics Letters, 70(10), p.1278, 1997.

Conferences - Refereed Full Papers in Proceedings:

1. M Nazzal, **S. Kaya**, T Gunay and P Ahmedzade, "Micro-Structural Characterization of Asphalt Nano-Composites", *2nd International Symposium on Asphalt Pavements & Environment – ISAP*, October 1-3, 2012, Fortaleza, Brazil.

2. M Nazzal, **S. Kaya**, Taylan Gunay and L Abu-Qtaish, "The Use of Nano-Mechanics Techniques to Evaluate the Effect of WMA on The Behavior of Asphalt Binders", *2nd International Symposium on Asphalt Pavements & Environment – ISAP*, October 1-3, 2012, Fortaleza, Brazil.

3. "Evaluation and Performance Analysis of Energy Efficient Wireless NoC Architecture", D DiTomaso, S Laha, **S Kaya**, A Kodi and D Matolak, *Proc. Int. 55th Midwest Symposium on Circuits and Systems – MWSCAS'55,* pp.798-801*,* 5-8 August 2012, Boise, ID, USA.

4. "A Closed form Memristor SPICE Model and Oscillator, I Abraham, S Kaya, G Pennington, *Proc. Int. 55th Midwest Symposium on Circuits and Systems – MWSCAS'55*, pp.1192–1195, 5-8 August 2012, Boise, ID, USA.

5. M Nazzal, **S. Kaya**, and L Abu-Qtaish, "Evaluation of WMA Healing Properties Using Atomic Force Microscopy", 7th RILEM International Conference on Cracking in Pavements, Delft, the Netherlands, Jun 20–22 June, 2012.

6. "Energy-Efficient Modulation for a Wireless Network-on-Chip Architecture" D DiTomaso, S Laha, **S Kaya**, D Matolak and A K Kodi 10th IEEE International NEWCAS Conference, - NEWCAS'10, Montreal, Canada, June 17-20, 2012.

7. "Optimum Biasing and Design of High Performance Double Gate MOSFET RF Mixers", S. Laha, M. Lorek and **S Kaya**, *International Symposium on Circuits and Systems – ISCAS,* 20-23 May 2012, Seoul, Korea.

8. "Double Gate MOSFET Based Efficient Wide Band Tunable Power Amplifiers", S Laha, **S Kaya**, A Kodi and D Matolak, *13th Wireless Microwave Technology Conference – WAMICON,* 15-17 April 2012, Cocoa Beach, FL, USA.

9. "iWISE: Inter-router Wireless Scalable Express Channels for Network-on-Chips (NoCs) Architecture," D DiTomaso, A Kodi, **S Kaya**, D Matolak, *IEEE 19th Annual Symposium on High Performance Interconnects – HOTI*, pp.11-18, 24-26 Aug. 2011, Santa Clara, USA.

10. "On Tunable Compact Analog Circuits with Nanoscale DG-MOSFETs", **S Kaya** and H F A Hamed, *Proc. Int. 53rd Midwest Symposium on Circuits and Systems – MWSCAS'53* 1-4 August 2010, Seattle, WA, USA.

11. "Studies of Ni and Co doped amorphous AlN for magneto-optical applications", W. M. Jadwisienczak, H. Tanaka, M. Kordesch, A. Khan, **S. Kaya**, R. V. Vuppuluri, *MRS Fall 2009*, Nov 30-Dec 4, Boston, MA, USA

12. "A Novel Voltage-Controlled Ring Oscillator Based on Nanoscale DG-MOSFETs", **S Kaya** & A Kulkarni, *20th IEEE Int. Conf. on Microelectronics - ICM'08*, 14-17 December 2008, Dubai, UAE.

13. "Low-Voltage Tunable Double-Gate MOSFET Transconductor for VHF/UHF Continuous-Time Filters", H F A Hamed and **S Kaya**, *19th IEEE Int. Conf. on Microelectronics - ICM'07* 29-31 December 2007, Cairo Egypt.

14. "Low-power tunable nanocircuits with DG-MOSFETs for current sensing applications, **S Kaya** and H F A Hamed, *SPIE Prooceedings 6769 – Nanosensing: Materials, Devices, and Systems III*, 9-12 September 2007, Boston, MA, USA

15. "Low Voltage Programmable Double-Gate MOSFETs Current Mirror and its As Programmable-Gain Current Amplifier", H F A Hamed, **S Kaya**, *14th IEEE Int. Conference on Electronics, Circuits and Systems - ICECS'07*, 11-14 December, 2007, Marrakech, Morocco.

16. "Models, Electrostatics and Molecular Dynamics of the Na+/K+-ATPase", J F Fonseca, R F Rakowski and **S Kaya,** Ohio *Collaborative Conference on Bioinformatics – OCCBIO 2006*, 28-30 Jun 2006, Athens, OH, USA. http://www.occbio.org

17. "A Novel Single-Gated Strained CMOS Architecture: COSMOS", A Al-Ahmadi and **S Kaya**, *Int. Conference on Simulation of Semiconductor Process and Devices – SISPAD*, 1-3 Sep 2005, Tokyo, Japan.

18. "Study of RF Performance for Graded-Channel SOI MOSFETs", W Ma and **S Kaya**, *Int. Conference on Simulation of Semiconductor Process and Devices – SISPAD*, 1-2 Sep 2005, Tokyo, Japan.

19. "Scaling of RF Linearity in DG and SOI MOSFETs", W Ma, **S Kaya**, and A Asenov, 11*th IEEE Int. Symposium on Electron Devices for Microwave and Optoelectronic Applications – EDMO*, 17-18 Nov 2003, Orlando, FL, USA.

20. "Enhanced Velocity Overshoot and Transconductance in Si/Si0.64Ge0.36/Si p-MOSFETs - Predictions for Deep Submicron Devices", M Palmer, G Braithwaite, M J prest, T E Whall, E H C Parker, Y P Zhao, **S Kaya**, J R Watling, A Asenov, J R Barker,A Waite and A G R Evans , *Proc. of 31st European Solid-state Device Research Conference – ESSDERC*, 11-13 Sep 2001, Nunberg, Germany.

21. "Analysis of Statistical Fluctuations due to Line Edge Roughness in sub-0.1mm MOSFETs", **S Kaya**, A R Brown, A Asenov, D Magot and T Linton*, Int. Conference on Simulation of Semiconductor Process and Devices – SISPAD*, 5-8 Sep 2001, Athens, Greece.

22. "Single stage amplifiers on a CMOS grade silicon substrate using a polymer interlayer dielectric with strained silicon MOSFETs" G Ternent, D L Edgar, E H McLelland, F Williamson, N Ferguson, **S Kaya**, C D W Wilkinson, I G Thayne, K Fobelets, J Hampson, *Asia-Pacific Microwave Conference*, p.767, 3-6 Dec 2000, Sydney, Australia.

23. "Indication of Non-equilibrium Transport in SiGe p-MOSFETs" Y P Zhao, **S Kaya**, J R Watling, A Asenov, J R Barker, M Palmer, G Braithwaite, T E Whall, E H C Parker, A Waite and A G R Evans, Proc. of 30th *European Solid-state Device Research Conference - ESSDERC*, p.224, 11-13 Sep 2000, Cork, Ireland.

24. "Metal Gate Strained Silicon SiGe MOSFETs for Microwave Integrated Circuits", G Ternent, D L Edgar, H McLelland, S Ferguson, **S Kaya**, C D W Wilkinson and I G Thayne *8th IEEE Int. Symposium on Electron Devices for Microwave and Optoelectronic Applications – EDMO*, 13-14 Nov 2000, Glasgow, Scotland.

25. "Effect of Oxide Interface Roughness on the Threshold Voltage Fluctuations in Decanano MOSFETs with Ultrathin Gate Oxides" A Asenov and **S Kaya**, *Int. Conference on Simulation of Semiconductor Process and Devices – SISPAD*, 5-8 Sep 2000, Seattle, USA.

26. "RF Analysis Methodology for Si and SiGe FETs Based on Transient Monte Carlo Simulation", S Roy, **S Kaya**, A Asenov and J R Barker, *Int. Conference on Simulation of Semiconductor Process and Devices – SISPAD*, 6-8 Sep 1999, Kyoto, Japan.

Conferences - Refereed Posters & Talks - Abstracts only:

1. "A SPICE Compatible Model for the Memristor", I Abraham, **S Kaya**, and G Pennington, IEEE Workshop on Microelectronics and Electron Devices – *WMDE'2012*, 22-25 May, 2012, Boise, ID, USA.

2. I Abraham, **S Kaya**, and G Pennington, "Diffusion based Memristor Compact Model", *Int. Workshop of Computational Electronics – IWCE'15*, 22-25 May, Madison, WI, USA, 2012

3. S. Laha, K.C. Wijesundara, A. Kulkarni, **S Kaya**, Ultra-Compact Low-Power ICO/VCO Circuits with Double Gate MOSFETs, *IEEE International Semiconductor Device Research Symposium – ISDRS*, 7-9 Dec 2011, Washington DC, USA.

4. "Temporal and Steric Analysis Of Ionic Permeation and Binding in Na^+,K^+-ATPase via Molecular Dynamic Simulations", J E Fonseca and **S Kaya**, *Biophysical Journal*, vol.96, Issue 3, 145a. Abstract submitted to the *Biophysical Society Meeting*, 28 Feb-4Mar, 2009, Boston, MA, USA.

5. "Highly Reconfigurable and Error Tolerant Threshold Logic Gates Based on Nanoscale DG-MOSFETs", **S Kaya**, D T-Y Ting and H F A Hamed, *International Semiconductor Device Research Symposium – ISDRS*, 9-11 Dec 2009, Washington DC, USA.

6. "Study of Ion-Motive ATPase Proteins for Multi-Valued Logic and Storage "J E Fonseca, K Clark, S-W Hla, R F Rakowski and **S Kaya**, *NSF EMT Workshop,* 24-25 July, 2008, Princeton, NJ, USA

7. "Nanocircuits for Sensors and On-Chip Analog Signal Processing", A Kulkarni and **S Kaya**, *Int. Conf. on Nanoscale Spectroscopy & Nanotechnology 5 – NSS5*, 15-19 Jul7, 2008, Athens, OH, USA

8. "Design of Reconfigurable Threshold Logic Using DG-MOSFETs", **S Kaya** and F A Hamed, *12th Int. Workshop of Computational Electronics – IWCE'12*, 08-10 October, 2007, Amherst, MA, USA

9. "Ion Permeation and Binding in Biomolecular Ion Pumps via Molecular Dynamics ", J E Fonseca, R F Rakowski, and **S Kaya**, *12th Int. Workshop of Computational Electronics – IWCE'12*, 08-10 October, 2007, Amherst, MA, USA

10. "Reconfigurable Threshold Logic Gates with nano-scale DG-MOSFETs", **S Kaya**, and H F A Hamed, *Nano Giga Challenges in Electronics and Photonics*, 12-14 March 2007, Phoenix, AZ, USA

11. "Compact Tunable Current-Mode Analog Circuits Using DG-MOSFETs", H Hamed, **S Kaya**, and J Starzyk, *2006 IEEE Int. SOI Conference*, 2-5 October, 2006, Niagara Falls, NY, USA.

12. "Modeling of Binding Sites and Electrostatics in the Ion-Motive Sodium Pump", J F Fonseca, **S Kaya**, R F Rakowski and S Guennoun, *6th IEEE Conference on Nanotechnology – IEEENano 2006*, 16-20 July, 2006, Cincinnati, OH, USA

13. "Low-Power Tuneable Analog Circuit Blocks Based on Nanoscale Dual-Gate MOSFETs", **S Kaya**, H Hamed and J Starzyk, 6th IEEE Conference on Nanotechnology – IEEE Nano 2006, 16-20 July, 2006, Cincinnati, OH, USA

14. "Power•Delay Product in COSMOS Logic Circuits", A Al-Ahmadi and **S Kaya**, *11th Int. Workshop of Computational Electronics – IWCE'11*, 25-27 May, 2006, Vienna, Austria.

15. "Electrostatic Modeling of Ion Motive Sodium Pump", J F Fonseca, **S Kaya**, and R F Rakowski, *11th Int. Workshop of Computational Electronics – IWCE'11*, 25-27 May, 2006, Vienna, Austria.

16. "Prediction of the location of binding sites in homology models of metal and alkaline-earth ion binding proteins", Reddy C , J F Fonseca, S Guennoun, **S Kaya** and R F Rakowski., *Swiss Biomedical Research Meeting - USGEB* , 23-24 Feb 2006, Geneva, Switzerland.

17. "Layout and Geometry Tolerances in COSMOS", A Al-Ahmadi and **S Kaya**, *International Semiconductor Device Research Symposium – ISDRS*, 6-9 Dec 2005, Washington DC, USA.

18. "Study of Dual-Gate SOI MOSFETs as RF Mixers", Swetha Varadharajan and **S Kaya**, International Semiconductor Device Research Symposium – ISDRS, 6-9 Dec 2005, Washington DC, USA.

19. "Homology Study of Na,K ATPases Based on SERCA ", J F Fonseca, **S Kaya** and R F Rakowski, *Mechanisms Of Membrane Transport – A Gordon Research Conference*, 5-10 June, 2005, Tilton, New Hampshire, USA.

20. "Device Scaling in COSMOS Architecture", A Al-Ahmadi and **S Kaya**, IEEE 63rd Device Research Conference – *DRC'63*, 20-22 June, 2005, Santa Barbara, California, USA

21. "Electro-Chemical Modeling Challenges of Biological Ion Pumps", R F Rakowski, **S Kaya** and J F Fonseca, *10th Int. Workshop of Computational Electronics – IWCE'10*, 24-26 Oct, 2004, West Lafayette, Indiana, USA.

22. "Search for Optimum and Scalable COSMOS", **S Kaya** and A Al-Ahmadi, *10th Int. Workshop of Computational Electronics – IWCE'10*, 24-26 Oct, 2004, West Lafayette, Indiana, USA.

23. "RF Performance of Strained SiGe pMOSFETs: Linearity and Gain", W Ma and **S Kaya**, *10th Int. Workshop of Computational Electronics – IWCE'10*, 24-26 Oct, 2004, West Lafayette, Indiana, USA.

24. "Simulation of Interface Roughness in DGMOSFETs using Non-Equilibrium Greens Functions", J Fonseca and **S Kaya**, IEEE 62nd Device Research Conference – *DRC'62*, 21-23 June, 2004, South Bend, Indiana, USA

25. "COSMOS: A New MOS Device Device Paradigm", **S Kaya***, Silicon Nanoelectronics Workshop – VLSI Symposia*,13-14 Jun 2004, Honolulu, Hawaii,USA.

26. "Simulation of Interface Roughness in DG-MOSFETs using Non-Equilibrium Green's Functions", J Fonseca and **S Kaya**, IEEE 34th SISC, 04-06 Dec, 2003, Washington, DC.

27. "Impact of Device Physics on DG and SOI MOSFET Linearity*",* W Ma and **S.Kaya***, Int. Semiconductor Device Research Symposium -ISDRS*, 10-12 Dec, 2003, Washington, DC.

28. J Fonseca and **S.Kaya**, "Accurate Treatment of Interface Roughness in Nanoscale DGMOSFETs using Non-Equilibrium Green's Functions"*, Int. Semiconductor Device Research Symposium - ISDRS*, 10-12 Dec, 2003, Washington, DC

29. "Design of DG-MOSFETs for High Linearity Performance", **S.Kaya**, W Ma and A.Asenov, *,IEEE Int. SOI Conference*, Sep 2003, Newport Beach, California, USA.

30. "Electro-thermal Analysis of RF Linearity in DG and SOI MOSFETs", W Ma and **S.Kaya**, *4th OSC Graduate Student Workshop and Conference*, 07-08 Aug 2003, Ohio Supercomputer Center, Columbus, Ohio, USA.

31. "Accurate Treatment of Interface Roughness in Nanoscale MOSFETs using Non-Equilibrium Green's Functions", J Fonseca and **S.Kaya**, *4th OSC Graduate Student Workshop and Conference*, 07-08 Aug 2003, Ohio Supercomputer Center, Columbus, Ohio, USA.

32. "Study of RF Linearity in sub-50nm MOSFETs Using Simulations", W Ma, **S.Kaya** and A.Asenov, *, 9th Int. Workshop of Computational Electronics – IWCE'9*, 26-29 May 2003, Frascati, Rome, Italy.

33. "Breakdown of Universal Mobility due to Atomistic Interface Considerations in nano-MOSFETs", **S Kaya** and A Asenov, *4th Motorola Workshop on Computational Materials and Electronics*, 14-15 Nov 2002, Tempe, AZ, USA.

34. "Breakdown of Universal Mobility Curves in sub-100nm MOSFETs", **S Kaya**, A Asenov and S. Roy*, Silicon Nanoelectronics Workshop – VLSI Symposia*,9-10 Jun 2002, Honolulu, HI,USA.

35. "Implications of Imperfect Interfaces and Edges in Ultra-small MOSFET Characteristics", A Asenov, **S Kaya** and A R Brown, *3rd Motorola Workshop on Computational Materials and Electronics*, 12-14 Nov 2001, Tempe, AZ, USA.

36. "On the breakdown of Universal Mobility Curves: A 3D Statistical Simulation Framework", **S Kaya**, A Asenov and S. Roy*, 8th Int. Workshop of Computational Electronics – IWCE'8*, Oct 2001, Urbana-Champaign, IL,USA.

37. 3D Modelling of Imperfect Interfaces and Edges in MOSFETs, **S Kaya**, A Brown, S. Roy and A Asenov, *Quantum Transport Workshop*, 17-22 June 2001, Maratea, Italy.

38. "Statistical 3D Simulation of Line Edge roughness in Decanano MOSFETs", A Brown, **S Kaya**, A Asenov, J H Davies and T. Linton, *Silicon Nanoelectronics Workshop – VLSI Symposia*,10-11 Jun 2001, Kyoto, Japan.

39. "Drift Diffusion and Hydrodynamic Simulations of Si/SiGe p-MOSFETs", Y P Zhao, J R Watling, **S Kaya**, A Asenov and J R Barker, *5th IUMRS Int. Conference on Advanced Materials*, 13-18 Jun 1999, Beijing, China.

40. "Monte Carlo Investigation of Optimal Device Architectures for SiGe FETs", S Roy, **S Kaya**, S Babiker, A Asenov and J R Barker, *6th Int. Workshop of Computational Electronics – IWCE 6*, Oct 1998, Osaka, Japan.

41. "Velocity Overshoot in psuedomorphic $Si_{0.8}Ge_{0.2}$p-MOSFET's", G Ansaripour, G Braithwaite, E H C Parker and T E Whall, **S Kaya**, Y-P Zhao, J R Watling, A Asenov, J R Barker, *8th European Heterostructure Technology Workshop*, 13-15 Sep 1998, Cardiff, UK.

42. "Strained Si/SiGe Quantum Wells and Wires on Vicinal (118) Si Substrates", **S Kaya**, T J Thornton, K Fobelets, P W Green and J M Fernandez, *Silicon Nanoelectronics Workshop – VLSI Symposia,* 8-9 Jun 1997, Kyoto, Japan.

Invited Talks:

1. "Nanoscale Transistors: Speed or Talent?", **S Kaya**, UC Davis, 17 November 2006, Davis, CA, USA.

2. "DG-MOSFETa for Reconfigurable and Tunable Nanocircuits ", **S Kaya**, University of Cincinnati, 2 February 2007, OH, USA.

3. "Nanotechnology & Energy: Solutions for 21st Century ", **S Kaya**, Turkish-American Society of Ohio, Academics Meeting, 8 January 2012, Columbus, OH, USA.